

N1085-90179

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## FACSIMILE TRANSMITTAL SHEET

In re application of: **Yeu-Der Chih**Examiner: **Huan Hoang**Serial No.: **10/785,522**Group Art Unit: **2827**Filed: **02/24/2004**Confirmation No.: **8308**

For: **AN ARRAY STRUCTURE OF TWO TRANSISTOR CELLS WITH MERGED  
FLOATING GATES FOR BYTE ERASE AND RE-WRITE IF DISTURBED  
ALGORITHM**

TO: Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

FACSIMILE NUMBER: 571-273-8300

## CONFIRMATION

## TELEPHONE:

FROM: Mark J. Marcelli

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DATE: October 12, 2005

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(INCLUDING COVERSHEET)

MESSAGE: **RE: RESPONSE TO OFFICE ACTION DATED AUGUST  
24, 2005**

NOTE: Original will not follow

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Appl. No. 10/785,522  
Amdt. dated 10/12/2005  
Response to Office Action of 08/24/2005

Attorney Docket No.: N1085-90179  
TSMC 2002-0115

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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Traci A. Gerard

Examiner Huan Hoang  
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P.O. Box 1450  
Alexandria, VA 22313-1450

**RESPONSE TO OFFICE ACTION DATED AUGUST 24, 2005**

Sir:

Responsive to the Office Action dated August 24, 2005, please re-examine and reconsider the above-identified application according to the amendments and remarks provided.

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks/Arguments** begin on page 11 of this paper.